



Advanced Encoder and Decoder Configurations and Features

Your CDQPrima contains a vast array of advanced features not available in any other codec.

4. Advanced Encoder and Decoder Features

Your **CDQPrima** comes standard with several advanced features that enable you to achieve the most from your codec applications. These features include digital audio I/O with built-in rate adaptation, standard on all models except the 110. Other features include peak and silence detection, advanced error concealment, sine detection, header and status bits and instantaneous A/D and D/A calibration. Other encoder and decoder features, such as status bits and simulated switches are used in conjunction with Prima Logic Language and will be discussed in that chapter.

4.1 Digital Audio Input and Output

<Encoder><Audio src>	EAI		Set encoder audio input source
<Encoder><More><General><Timing>	ETI		Set encoder digital audio timing
<Decoder><AES><Output SR>	DDO		Set decoder digital audio output sampling rate
<Decoder><AES><Sync>	DES		Enable decoder AES sync timing
<Decoder><AES><TimingSrc>	DTI	N/A	Set decoder output timing sync source

AES/EBU and S/PDIF digital audio input and output is either standard or available on all **CDQPrima** models. All 200 Series models have gold plated, industry standard XLR connectors for digital audio I/O. Due to rear panel space limitations, 100 Series models have a DB9 connector, and require an adapter cable, available from MUSICAM USA, as shown in Appendix A.

To activate digital audio input, use the **EAI** command or the menu command sequence

<Encoder><Audio Src>.

Using this command, you can instantly toggle between two audio sources. You can even control the audio source from the far end or by using Prima Logic Language. The digital audio output is always enabled, as is the analog audio output.

4.1.1 Selecting AES/EBU or S/PDIF Digital Audio

The same connectors are used for both AES/EBU and S/PDIF input and output. The digital I/O level settings are changed with jumpers on the main circuit board. Unless otherwise requested, the **CDQPrima** is shipped from the factory strapped for professional AES/EBU I/O. To change these settings, remove the power cord and carefully remove the top of the **CDQPrima**. Three jumpers, P5, P9 and P10 are located between the power supply and the rear panel. When the jumpers are in position 'P', the **CDQPrima** is set for professional AES/EBU digital input and output. Moving the jumpers to the 'C' position sets the **CDQPrima** for consumer-grade S/PDIF digital I/O.

It is not necessary to set the digital audio input, output and sync to the same format. You can input consumer grade S/PDIF audio and output professional grade AES/EBU audio.

4.1.2 Digital Audio Timing

Please note that digital audio input and output is not supported when using the G.722 algorithm

The digital audio is rate adapted on input as well as output to eliminate any digital clock problems. The AES/EBU or S/PDIF digital output from the decoder can be synchronized to a studio clock through an external sync input located on the rear of the **CDQPrima**.

Because of the rate adapters, the input/output digital clock rates are not required to be the same as the internal clock rates. For example, it is

possible to input 44.1 kHz AES/EBU digital audio and ask the **CDQPrima** to perform compression at 48, or 32 kHz rates (by using the front panel LCD display or the remote control **ESR** command). **CDQPrima** encoder does not use 44.1 kHz compression.

Digital audio input sources can be 32, 44.1 or 48 kHz, all industry standards. These input sampling rates are automatically sensed and rate adapted by the **CDQPrima**. 32, 44.1, or 48 kb/s output sampling can be achieved using internal clocking. In addition, an external clock source can be provided to the SYNC input to lock the digital input rate and output sampling to the studio clock.

The digital audio sampling rate should not be confused with the encoder/decoder sampling rate. These are two different parameters. Digital audio output sampling rate is set using the **DDO** command or by an external sync source. Encoder sampling rate is set using the **ESR** command. Decoder sampling rates is slaved to the encoder rate and no setting is possible or needed.

The compression sampling rate at the encoder determines the digital sampling rate at the decoder. Thus the encoder sample rate of the far-end codec sets the internal sampling rate of the decoder. The AES/EBU or S/PDIF digital output sampling rate at the decoder is determined by the **DDO** command and can be a variety of values. The digital audio output sampling rate is independent of the encoder/decoder sampling rate, with restrictions.

The encoder receives direct digital input by way of the connector on the rear panel. Analog or digital (but not both simultaneously) signals may be input to the **CDQPrima** as selected during encoder setup. If the digital input is selected, the **CDQPrima** locks to the incoming digital audio input and displays the lock condition on a front panel LED (Models 120, 220 and 230 only). If digital audio input is selected, the AES PLL lock light must be illuminated before audio is accepted for encoding. In normal operation, the **CDQPrima** locks its internal clocks to the clock of the telephone network. For loopback, it locks its clocks to an internal clock. In either case, the clock used by the **CDQPrima** may not be at precisely the same frequency as the AES/EBU or S/PDIF input. To prevent slips from occurring due to the presence of two master clocks, a rate synchronizer is built into the encoder section to perform the necessary rate conversion between the two clocks.

The decoder provides digital signals by way of the rear panel connector(s). Additionally, the decoder may be synchronized to an external clock through the SYNC connector on the rear panel (or the SYNC connector of the adapter cable). If no input is present on the decoder SYNC input line, then the output digital audio timing is generated by the internal clock source that is either at the ISDN or internal clock rate. If the SYNC input is present, then digital audio

presence of a valid sync source is indicated by the illumination of the front panel AES PLL LED (on Models 120, 220 and 230). The sync source, and again rate synchronization is performed to prevent any

assumed to be an AES/EBU or S/PDIF signal with or without data present. The **Prima** sync determination.

The timing controlled by various **CDQ rima** commands. The encoder timing, **ETI** command or the <Encoder><More><General><Timing>,

input timing from the audio source and Internal derives the timing from **Prima** the **CDQ rima**'s sync input for digital timing. This allows slightly off-

The decoder timing is derived in four different ways. These modes of timing **DTI** command (click on the Decoder icon from the

<Decoder><AES><TimingSrc>

and are:

- NORMAUTO
INTAUTO
INT
AES

NORMAUTO mode of timing. In this mode of

D/A converter and the AES/EBU transmitter for the sampling rates of 48 and 32 kHz. For the sampling rates of 24 and 16 kHz, the decoder transmitter. Table 4-1 shows the configurations.

Decoder Sampling Rate kHz	Rate Adaption Used	Digital Audio Output Sampling Rate kHz
48	NO	48
48	YES	44.1
48	YES	32
48	YES	29.5
32	YES	48
32	YES	44.1
32	NO	32
32	YES	29.5
24	YES	32
16	YES	29.5

Table 4-1 Decoder rate adaption for NORMAUTO

The block diagram of the timing is shown in Figure 4-1 for the non-rate-adapted and figure 4-2 for the rate-adapted case.

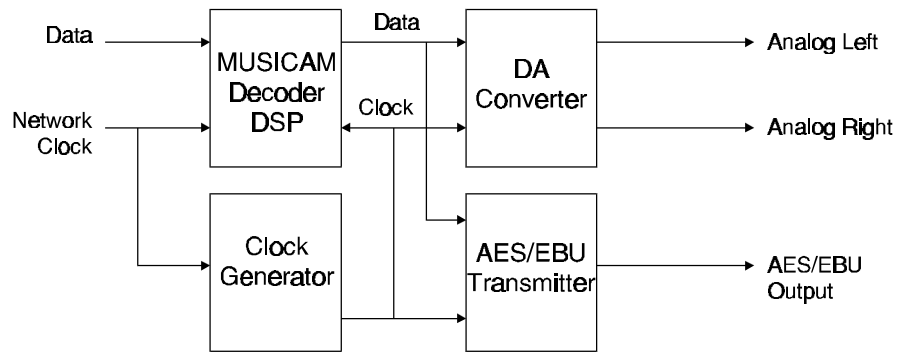


Figure 4-1 Decoder output timing with AES/EBU sync disabled or not present using NORMAUTO timing with no rate adaption

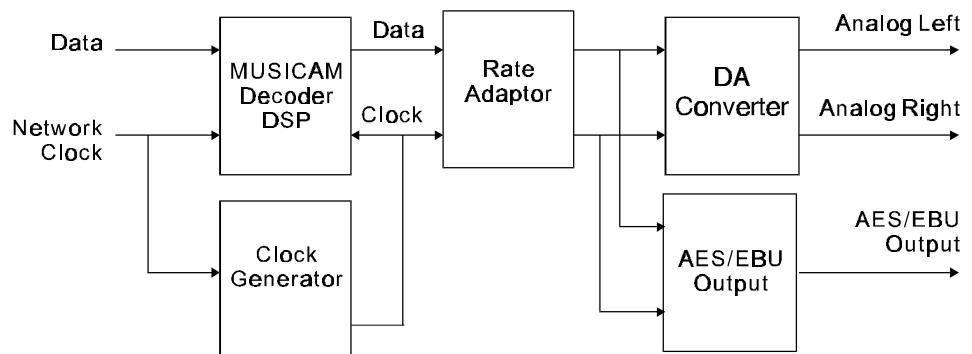


Figure 4-2 Decoder output timing with AES/EBU sync disabled or not present using NORMAUTO timing with rate adaption or INTAUTO timing

For DTI set to INTAUTO, a rate adapter is used in all cases, as shown in Figure 4-2. The operational table for this mode is shown below:

Decoder Sampling Rate kHz	Rate Adaption Used	Digital Audio Output Sampling Rate kHz
48	YES	48, 44.1, 32, 29.5
32	YES	48, 44.1, 32, 29.5
24	YES	44.1, 32, 29.5
16	YES	29.5

Table 4-2 Decoder rate adaption for INTAUTO

If DTI is set to INT, then rate adaption is always used and the DDO command is used to set the output sampling rate. Care must be taken when utilizing the DDO command to set the sampling rate, because not all combinations of rates are possible. See the DDO command in the *CDQPrima Remote Control Manual* for the table of possibilities. Figure 4-3 shows internal timing.

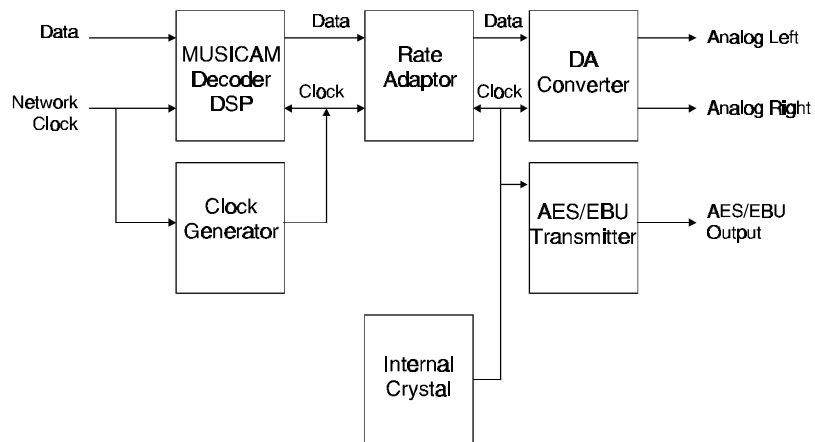


Figure 4-3 Decoder output timing with AES/EBU sync disabled, using INT timing or rate adaption

If DTI is set to AES, the output sampling rate is determined by the AES sync input, as shown in Figure 4-4. This insures that digital audio outputs are in sync with digital audio all external digital audio equipment. The decoder sync input may or may not be available. The

DES command is used to control the timing requirement for the sync input.

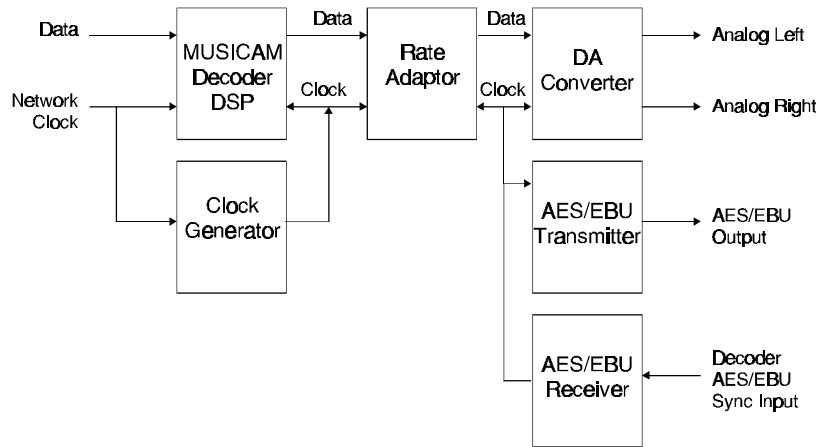


Figure 4-4 Decoder output timing using AES/EBU sync source enabled and AES timing

4.1.3 Operation at 44.1 kHz Sampling Rate

The **CDQPrima** allows operation at various digital audio sampling rates. See Fig. 4-5 for reference. Please do not confuse digital audio sampling rates with compressed audio (encoder and decoder) sampling rates. The digital audio input signal is usually 44.1 kHz for consumer audio applications such as CD players. This input signal may also be 48 or 32 kHz if the input source is a professional device such as a DAT. The input signal is then rate adapted before entering the compressed audio encoder. The output of the rate adaptor is usually 48 kHz or 32 kHz. This digital audio output sample rate is selected at the decoder and does not have to be the same as the digital audio input sample rate. 44.1 kHz digital audio output is available but the decoded audio must be rate adapted to achieve this output rate. The encoder rate adapter sampling rate is set by the **ESR** command. In Fig. 4-5, the normal case of 48 kHz is shown. The **CDQPrima** can accept 44.1 digital audio signals even if it operates at a compression sampling rate of 48 kHz.

The compressed audio signal is then transmitted to the decoder where it is de-compressed with an output sampling rate which is the same as the *encoder* sampling rate (not necessarily the same as the input sampling rate). In this case, it is 48 kHz. The decoder output is then rate adapted to the desired sampling rate for external use. The decoder rate adapter sampling rate is set by the **DDO** command and can be 48, 44.1 or 32 kHz.

Note that the output digital audio sampling rate is independent of the input audio sampling rate and the encoded sampling rate. This allows ultimate flexibility. The output sampling rate is completely arbitrary.

The encoder sampling rate (set by the **ESR** command) should be set the same or higher than the input sampling rate to insure that there is no bandwidth reduction. The compression algorithms work better at lower sampling rates, so the encoder sampling rate should be set only slightly higher the input sampling rate.

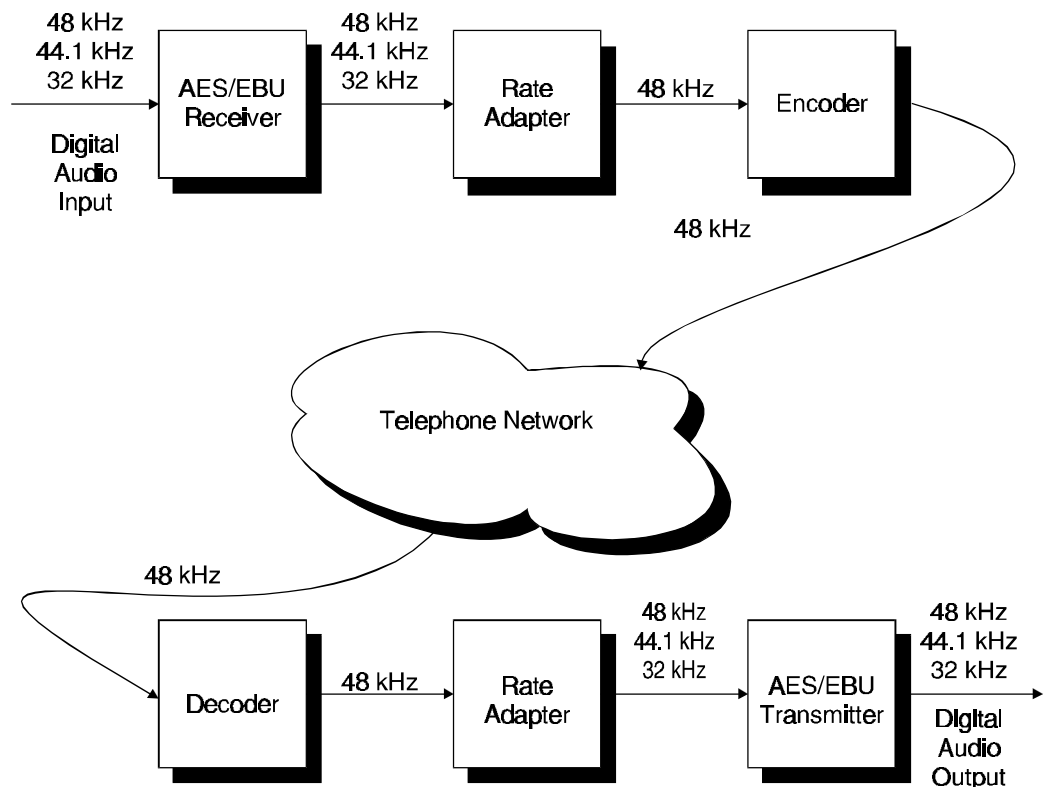


Figure 4-5 AES/EBU or S/PDIF input and output

4.2 Peak Level Detection

All **CDQPrima** Models, including those without level meters, come with 6 built-in peak level detectors. These allow the user to set the correct input level to maximize signal-to-noise ratios without overloading either the encoder or decoder stages. The six detectors are encoder left, encoder right, encoder stereo, decoder left, decoder right and decoder stereo.

The peak detectors remember the highest input level since the last reset, and display this level when accessed. Accessing the peak level resets the memory. The keypress sequence

<Maint><Peak Det><Peak Lvl>

or the **MPD** commands are used to display and reset the peak level.

4.3 Quiet Detection / Audio Detection

One of the most powerful features of the **CDQPrima** is the availability of six silence detectors. The silence detectors, coupled with Prima Logic Language make automatic, unattended operation possible for applications such as STL backup and others.

<Maint><Quiet Det><Time left>	MQC	N/A	Display silence detector level time remaining
<Maint><Quiet Det><Read lvl>	MQD	N/A	Display silence detector level
<Maint><Quiet Det><Set lvl>	MQL	N/A	Set silence detector level
<Maint><Quiet Det><Set time>	MQT	N/A	Set silence time duration

There are six silence detectors¹. These are:

- Encoder left channel input
- Encoder right channel input
- Encoder stereo input
- Decoder left channel output
- Decoder right channel output
- Decoder stereo output

A stereo silence detector uses the greater of the left or right channel signal for the determination of silence.

At 0.1 second intervals, the audio levels of the encoder and decoder left and right channels are measured. If the level is below the value set by the **MQL** command

<Maint><Quiet Det><Set lvl>

for a period of time as set by the **MQT**

¹Throughout this manual, the terms 'Quiet Detector' and 'Silence Detector' are used interchangeably.

<Maint><Quiet Det><Set time>

command, then the channel is said to be silent. When a channel is silent, the silent event input is set to true. The value of the silence event may be used as input for the Event-to-Action logic interpreter and can initiate a PLL action or virtual action.

The current value of any of the six silence detectors can be displayed by the **MQD**



<Maint><Quiet Det><Read lvl>

command. The time remaining before a silence detection event can be displayed by the **MQC** command

<Maint><Quiet Det><Time left>.

Remembering that any event can be mapped into other events using Boolean operators, by simply NOTing a silence detector, you create an audio detector. Using this 'audio detector' is easy to make the **CDQPrima** execute any command, including dialing into a remote unit, on the presence of audio. Further discussions of and uses for quiet and audio detectors can be found the Prima Logic Language chapter of this reference.

4.4 Error Concealment

<Decoder><More><ACE>	DSP		Scale decoder scalefactor protection
<Encoder><More><General><ACE> >	ESP		Set encoder scale factor protection

Another MUSICAM USA exclusive feature available on all **CDQPrima** Models is Advanced Concealment of Errors (ACE). ACE is based on CRC (Cyclic Redundancy Code) protection of the ISO/MPEG Layer II scale factors.

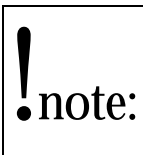
This feature is controlled by the **DSP**

<Decoder><More><ACE>

and **ESP**

<Encoder><More><ACE>

commands. In general, it is better to use scale factor protection if the data channel is noisy (high BER). Scale factor protection (**ESP**) is used for all ISO/MPEG Layer II types of bitstreams. Scale factors are the levels of the digital audio signal within a sub-band. There are 32 sub-bands and the scale factors change the level over a 120 dB range. An error on any scale factor will cause a perceptible impairment in the audio. To prevent this, scale factor protection can be inserted at the encoder and if the decoder is capable of recognizing it, then the decoder can perform a concealment operation to repair the damaged scale factor. If the decoder does not know about scale factor protection, the audio is decoded and any damaged scale factors cause an impairment.



Scale factor protection is *not* bi-directional, and must be enabled independently for each direction. **If ESP has enabled scale factor protection, the far end decoder must enable scale factor correction with the DSP command. If only one end has scale factor protection enabled, audio may be muted.** The *CDQPrima*'s Scale factor protection is not compatible with other manufacturers codecs. Scale factor protection is compatible with MUSICAM USA's CDQ2001 codec.

4.5 Sine Detection

<Encoder><More><General><Sine Det>	ESD	N/A	Set encoder sine wave detector
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Sine wave detection (**ESD**) should be used only when using test tones for audio analysis with test equipment, and should be OFF for normal operation.

4.6 Encoder Header and Decoder Status Bits

<Decoder><More><Stat bits>	DRS	N/A	Print real-time decoder status bits
<Encoder><More><ISO Hdr><Copyright>	ECR	Setup, ISO Header	Set encoder copyright bit in header
<Encoder><More><ISO Hdr><Emphasis>	EEP		Set encoder emphasis bit in header
<Encoder><More><ISO Hdr><Original>	EOR		Set encoder original bit in header
<Encoder><More><ISO Hdr><Protect>	EPR		Set encoder protection bit in header
<Encoder><More><ISO Hdr><Private>	EPI	N/A	Set encoder private bit in header


When using the CCSO, CCSN² or ISO/MPEG Layer II compatible audio compression algorithm, there are certain flags that may be set in the header. These bits can be used by the decoder or can be used as additional signaling paths.

These bits are defined below and the command used to set the bit is shown in parenthesis:

- Copyright (**ECR**)
- Emphasis (**EEP**)
- Original (**EOR**)
- Protection (**EPR**)
- Private (**EPI**)

The **DRS** command display the real-time decoder status bits for the ISO/MPEG algorithm. These status bits are also displayed by the **CST** command, along with other information. The status bits displayed are the ISO frame header bits that are set by the encoder (See Encoder Header, above).

4.7 A/D and D/A Calibration

<Decoder><More><Cal DA>	DDA	N/A	Calibrate D/A converter
<Encoder><More><General><Cal AD>	EAD		Calibrate A/D converter

The decoder Digital to Analog (D/A) converter can be calibrated by the **DDA** command. This calibration process assures that the D/A converter is operating optimally. The analog input A/D converter is calibrated by the **EAD** command. This calibration is performed automatically at power-up but can be manually performed at any time. The calibration process removes the effect of any DC voltage offset present at the input of the A/D converter. This has a minor positive effect on the audio compression algorithm. It may be beneficial to re-calibrate after an audio source has been changed.

²Some early production MUSICAM USA products using the MUSICAM[®] enhanced ISO/MPEG Layer II compression, were manufactured before the ISO standardized MPEG Layer II bit stream and header. The CCSO (CCS Old) algorithm will communicate with these devices manufactured before 1993. The CCSN (CCS New) algorithm will communicate with all MPEG Layer II devices that conform to the standard.